Amendments to the Specification:

Amend page 7, paragraph beginning at line 19 as follows:

In accordance with the preferred embodiment, the frame header 12 of Figure 2 includes one bit in the MC field, two bits in the ~~VFSH~~ VSHF field, and two bits in the ~~FHVF~~ FHEF field which are exemplary only. The egress processor 2 has associated with it a hardware classifier which detects from the data in these three fields a five-bit code (one bit from the MC field, two bits each from the VFSH and VHVF fields). The five-bit code identifies at least 32 starting addresses for 32 different sets of pico code to be executed by the egress processor.

Amend page 8, paragraph beginning at line 23 as follows:

Processor 8 executes an instruction set for processing the data stored in the frame input area (FIA) 6. The Forwarding Enque Area (FEA) 9 contains a list of ENQUE parameters, including well known frame alteration parameters (WFA) and flexible frame alteration parameters (FFA). Control structures are created for modifying the frame under control of the egress processor code. Processing of the frame is conventional in that search trees based on keys derived from the contents of the Frame Input Area (FIA) are created, and the results of that search produces other ENQUE parameters, as well as WFA and FFA which are stored in 9. Intermediate values obtained during these calculations are stored in the scratch memory ~~12~~ 19 and general purpose registers 10. Hardware assist

units 16 are also employed in the process for building the control structures in the Forwarding Enque Area.

Amend page 12, paragraph beginning at line 5 as follows:

The hardware frame classifier 18 includes a table which is indexed by the five bits input to the hardware frame classifier 18 from the foregoing MC, ~~VHSF~~ VSHF, FHEF fields. The five bits identify a starting address of the pico code instructions stored in the processor 8. Individual instructions following the starting address within the pico processor 8 may, in turn, look to the FHE fields, and VHE fields when the decoded output from the hardware frame classifier 18 points to the relevant set of instructions. For instance, when the FHE field is 10, a jump address is provided in the FHE field, which when the relevant instructions following the entry point of a set of instructions are executed, read the contents of the FHE field to obtain the jump instruction.